REMARKS

This Amendment responds to the non-final Office Action mailed on June 9, 2008. Claim 1, 3, 5-8, 15-19, 34, 35, 43, 44, 46-48, 52, and 53 are pending. Claims 9-13, 20, 36-42, and 49-51 are withdrawn. Claims 1, 5, 6, 36, 43, and 46 have been amended. In view of the following remarks, as well as the preceding amendments, Applicants respectfully submit that this application is in complete condition for allowance and request reconsideration of the application in this regard.

Rejection Under 35 U.S.C. § 112, 2nd Paragraph

Claims 1, 3, 5-8, 15-19, 34, 35, 43, 44, 46-48, 52, and 53 stand rejected under 35 U.S.C. § 112, 2nd Paragraph. Applicant has amended claims 1 and 43 in a manner sufficient for the Examiner to withdraw the rejection.

Rejections Under 35 U.S.C. § 103

Claims 1, 3, 5-8, 15-19, 34, 35, 43, 44, 46-48, 52, and 53 over Choi and Occhipinti

Claims 1, 3, 5-8, 15-19, 34, 35, 43, 44, 46-48, 52, and 53 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Choi et al. (U.S. Patent No. 6,566,704), hereinafter *Choi*, in view of U.S. Publication No. 2004/0027889 to Occhipinti et al. (hereinafter *Occhipinti*). Claims 1 and 43 are independent claims. Applicants respectfully traverse the rejection for the reasons set forth below.

Claim 1 sets forth "an interconnected plurality of semiconductor device structures arranged in an array characterized by a plurality of rows and a plurality of columns." The Examiner admits that Figure 3F of *Choi* fails to disclose that the device structures are arranged as

an interconnected plurality of semiconductor device structures in an array. However, the Examiner attempts to rely on Figure 4B of *Choi* to cure this deficiency.

Figures 4A and 4B of *Choi* teach that a device construction the gate electrode (20) and gate dielectric (30) are disposed in a layer stack above the nanotubes (100) with an overlying relationship. Hence, the gate dielectric (30) is not disposed on a sidewall of gate electrode (20). Moreover, Figures 4A and 4B of *Choi* also teach that the gate electrode (20) and gate dielectric (30) are separated from one end of each nanotube (100) by the drain (50) and, therefore, are suspended above the nanotubes (100). The channel region of each nanotube (100), which is between the source (40) and drain (50), is not disposed adjacent to a vertical sidewall of the gate electrode (20), as also required by Applicants' claim 1.

Applicants agree with the Examiner, as stated on page 9 of the June 9, 2008 Office Action, that Figure 3F in *Choi* teaches a gate electrode (30) disposed on a vertical sidewall of a gate electrode (20) and that Figure 3F in *Choi* teaches a channel region of the nanotube disposed adjacent to a vertical sidewall of the gate electrode (20). Applicants do not dispute these findings by the Examiner with regard to Figure 3F. However, in the Office Action, the Examiner is modifying the structure in Figure 3F based upon the teachings from Figure 4B in *Choi*. Applicants' following remarks pertain to that attempted modification, which is improper for multiple reasons.

However, *Choi* also teaches that, were one to attempt to modify the device structure shown in Figure 3F based upon the disclosure in Figures 4A and 4B, the gate electrode (20) must be moved in compliance with Figures 4A and 4B. After the move, each nanotube (100) no longer has a channel region disposed adjacent to a vertical sidewall of the gate electrode (20). Instead, the channel region of each nanotube in Figures 4A and 4B of *Choi* is located below the gate electrode (20). In addition, this attempted modification would require that the gate

dielectric (30) be moved so that it is no longer on a sidewall of the gate electrode (20). Instead, the gate dielectric (30) in Figure 3F would somehow have to be modified to be a layer in a layered stack that includes the gate electrode (20) as yet another layer in the layered stack. Furthermore, this attempted modification would require that the gate electrode (20), gate dielectric (30), and drain (50) be rearranged as shown in Figures 4A and 4B such that the gate electrode (20) and gate dielectric (30) are in a layered stack disposed above the drain (50), instead of between the drain (50) and the drain (40) as shown in Figure 3F. To satisfy the requirements to provide an interconnected plurality of semiconductor device structures as shown in Figures 4A and 4B, a person having ordinary skill in the art would have had to modify multiple additional features of the device structure in Figure 3F to the point that Figure 3F would no longer read on Applicants' claim 1.

Choi discloses at column 5, lines 1-3 that, in comparison with the embodiment shown in Figure 3E, "the second embodiment differs in that the gate 20 is formed between the source 40 and drain 50" and at column 4, lines 33-38 that Figures 4A and 4B show an embodiment that "is the same as the vertical nano-sized transistor according to the first embodiment except that a gate 20 is formed over a drain 50… ." A *prima facie* case of obviousness may be rebutted by showing that the art, in any material respect, teaches away from the claimed invention. This requirement for a different embodiment to provide an array of interconnected devices materially teaches away from modifying the device structure in Figure 3F as proposed by the Examiner.

On page 9 of the Office Action, the Examiner persists that "[t]he examiner does not suggest to rearrange the elements of the embodiment o *(sic)* figure 3F according to the embodiment of figure 4B of *Choi*. The embodiment of figure 4B is cited to merely teach an artisan that each of said semiconductor device structures is arranged as an interconnected

plurality of semiconductor device structures in an array characterized by a plurality of rows and a plurality of columns." However, this statement by the Examiner is not supported by any objective facts.

Applicants admit that forming transistors in an array is conventional. The Examiner's rejection fails to acknowledge the additional structural modifications that a person having ordinary skill in the art, armed with the teaching of Figure 4A of *Choi*, would have made to the device structure of Figure 3F of *Choi* in order to arrange a plurality of the devices structures depicted in Figure 3F as a plurality of interconnected device structures. Even *Choi* sets forth the single nanotube device structure in Figure 3 and the interconnected device structures in separate and distinct embodiments in its written description, which a person having ordinary skill in the art would have interpreted to mean that the intrinsic evidence in *Choi* itself fails to demonstrate that there would have been a reasonable expectation of success to make the modifications suggested by the Examiner. The sole source of such as teaching is Applicants' specification, which is improper. Absent the guidance from Applicants' specification, the Examiner is engaging in speculation.

Furthermore, according to MPEP § 2143, the prior art can be modified or combined to reject claims as *prima facie* obvious as long as there is a reasonable expectation of success. In this instance, a person having ordinary skill in the art would not have appreciated from the disclosure associated with Figures 4A and 4B of *Choi* that a reasonable expectation of success exists to modify the structure shown in Figure 3F *Choi* as proposed by the Examiner if this modification requires that the gate electrode (20) be relocated to an entirely different location in the device structure. As mentioned above, the specification of *Choi* itself recognizes that this modification proposed by the Examiner requires a wholesale rearrangement of the elements, including relocation of the gate electrode (20), gate dielectric (30), and drain (50), of the device

structure of Figure 3F. *See Choi* at column 4, line 34 to column 5, line 7. Hence, these are not obvious modifications that a person having ordinary skill in the art would have made to the device structure of Figure 3F with a reasonable expectation of success based on Figure 4B of *Choi* or any other source.

Occhipinti fails to remedy these deficiencies in *Choi*. For at least these reasons, Applicants submit that the Examiner has failed to properly support a case of *prima facie* obviousness with regard to claim 1. Therefore, Applicants respectfully request that the Examiner withdraw this rejection.

The Examiner states on page 10 of the Office Action that the reason allegedly permitting the modification to Figure 3F of Choi is "in order to use the device in a practical application which requires plurality of unit cells and in order to simplify the processing steps of making the device by using conventional rows and columns array matrix." This reasoning is not objective. In the Office Action, the Examiner's reasoning fails to address how the structure shown in Figure 3F of *Choi* can be modified to include multiple semiconducting carbon nanotubes and ignores other teachings in *Choi* itself.

Claim 1 is patentable for additional reasons.

Claim 1 also sets forth that each semiconductor device structure in the interconnected plurality of semiconductor device structures includes "a plurality of semiconducting carbon nanotubes having a channel region disposed adjacent to said vertical sidewall of said gate electrode." The Examiner admits on page 3 of the June 9, 2008 Office Action that the device structure in Figure 3F of *Choi* fails to disclose a plurality of nanotubes. However, the Examiner attempts to rely on Figure 4B of *Choi* to cure these deficiencies, as reflected at the bottom of page 3 of the Office Action. Figure 4B of *Choi* does disclose multiple nanotubes (100).

Choi states that Figure 1 shows "a unit cell of a vertically aligned carbon nanotube transistor." Therefore, Figure 1 of *Choi* shows a single nanotube (100) in the unit cell. *Choi* states that "FIG. 4B illustrates a perspective view of the vertical nano-sized transistor using carbon nanotubes shown in FIG. 4A, in which a source line and a drain line intersect at locations where the carbon nanotubes are grown to form unit cells." Based upon this disclosure, the most reasonable construction of Figures 4A, 4B in *Choi* is that multiple unit cells are shown; that each unit cell is defined at the intersection of a drain line and a source line so that each unit cell is a device structure in an interconnected plurality of device structures; and that each of the unit cells includes a single nanotube (100) extending between source and drain lines. Therefore, *Choi* fails to disclose a device construction in which each semiconductor device structure includes a plurality of semiconducting carbon nanotubes, as set forth in claim 1.

A *prima facie* case of obviousness requires that the references teach or suggest all the claim limitations. In this instance, *Occhipinti* fails to remedy the preceding deficiency of *Choi* in that *Occhipinti* also fails to disclose a device construction in which each of the semiconductor device structures includes a plurality of semiconducting carbon nanotubes. Accordingly, the Examiner has failed to establish a *prima facie* case of obviousness. For this additional reason, Applicants request that the Examiner withdraw the rejection.

On page 10 of the June 9, 2008 Office Action, the Examiner alleges in his remarks that "the above features are not recited in the rejected claim(s)." The Examiner's attention is directed to claim 1 that recites "each of said semiconductor device structures further including ... a plurality of semiconducting carbon nanotubes." Applicants fail to understand how these "features" are not recited in claim 1 and request clarification from the Examiner regarding this allegation.

Applicants' independent claim 43 is patentable for at least the same or similar reasons as independent claim 1. Specifically, claim 43 sets forth "a gate electrode including a vertical sidewall and a gate dielectric disposed on the vertical sidewall" and "a plurality of semiconducting carbon nanotubes extending substantially vertically adjacent to said vertical sidewall of said gate electrode." For at least this reason, Applicants respectfully request that the Examiner withdraw the rejection.

Because claims 3, 5-8, 15-19, 34, and 35 depend from independent claim 1 and claims 44, 46-48, 52, and 53 depend from independent claim 43, Applicants submit that these claims are also patentable for at least the same reasons discussed above. Furthermore, each of these dependent claims recites a unique combination of elements not disclosed or suggested by the combination of *Choi* and *Occhipinti*.

Claims 5, 6, 34, and 46 over Choi, Occhipinti, and Farnworth

Claims 5, 6, 34, and 46 stand rejected under 35 U.S.C. § 103(a) as being unpatentable *Choi* and *Occhipinti* further in view of Farnworth et al. (U.S. Patent No. 6,515,325), hereinafter *Farnworth*. Applicants have amended claims 5, 6, 34, and 46 to place the claims in a clarified form for the Examiner. Because claims 5, 6, and 34 depend from independent claim 1 and claim 46 depends from independent claim 43, Applicants submit that these dependent claims are patentable for at least the same reasons. Furthermore, these dependent claims recite unique combinations of elements not taught, disclosed or suggested by the combination of *Choi*, *Occhipinti*, and *Farnworth*.

Conclusion

Applicants have made a bona fide effort to respond to each and every requirement set forth in the Office Action. In view of the foregoing remarks and amendments, this application is submitted to be in complete condition for allowance. Accordingly, a timely notice of allowance to this effect is earnestly solicited. In the event that any issues remain outstanding, the Examiner is invited to contact the undersigned to expedite issuance of this application.

Applicants do not believe any fees are due in connection with filing this communication. If, however, any fees are necessary as a result of this communication, the Commissioner is hereby authorized to charge any under-payment or fees associated with this communication or credit any over-payment to Deposit Account No. 23-3000.

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Date

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